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HAVERSTOCK & OWENS LLP
260 Sheridan Avenue, Suite 420
Palo Alto, California 94306
(650) 833-0160

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NEW PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

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NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of Inventor: Gwilym Francis Luff et al.

Title: **NOVEL TOPOLOGY FOR A SINGLE ENDED INPUT DUAL BALANCED MIXER**

CERTIFICATION UNDER 37 CFR § 1.10

I hereby certify that this New Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date, November 22, 2000, in an envelope bearing "Express Mail Post Office To Addressee" Mailing Label Number EL703212555US addressed to: **PATENT APPLICATION**, Assistant Commissioner for Patents, Washington, D.C. 20231.

Tadas Narauskas
(Name of Person Mailing Paper)

Tadas Narauskas
Signature

Enclosed are:

1. The papers required for filing date under CFR § 1.53(b):

   26 Pages of Specification (including claims); 7 Sheet(s) of Drawings.
   X Formal
   _ Informal

2. X Declaration or Oath (executed by Gwilym Luff)
3. _ Power of Attorney by Assignee
4. _ Assignment of the Invention to Micro Linear Corporation (including Form PTO-1595).
5. Fee Calculation

   _ Amendment changing number of claims or deleting multiple dependencies is enclosed.

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Basic Fee
				$710.00
Total Claims	21 - 20 =	1	$18.00	18.00
Independent Claims	6 - 3 =	3	$80 00	240.00
Multiple Dependent claim(s), if any			$270.00	
			Filing Fee Calculation	$968.00

6. X Applicants qualify for Small Entity Status

   50% Filing Fee Reduction (if applicable) $484.00

7. Other Fees

   _ Assignment Recordation Fee

   _ Other 0.00

   TOTAL FEES ENCLOSED **$484.00**

8. Payment of Fees

   X Check in the amount of $484.00 enclosed.

9. X Authorization to Charge Additional Fees

   The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.16 or § 1.17 to Account No. 08-1275. **An originally executed duplicate of this transmittal is enclosed for this purpose.**

10. _ Information Disclosure Statement
11. X Return Receipt Postcard

Dated: November 22, 2000

By: Thomas B. Haverstock
Name: Thomas B Haverstock
Registration No.: 32,571

PATENT
Atty. Docket No. MLNR-08101

NOVEL TOPOLOGY FOR A SINGLE ENDED INPUT DUAL BALANCED MIXER

Related Applications:

This application claims priority under 35 U.S.C. § 119(e) of the co-pending U.S. provisional application Serial Number 60/167,188 filed on November 23, 1999 and entitled "NOVEL TOPOLOGY FOR A SINGLE ENDED INPUT DUAL BALANCED MIXER." The provisional application serial number 60/167,188 filed on November 23, 1999 and entitled "NOVEL TOPOLOGY FOR A SINGLE ENDED INPUT DUAL BALANCED MIXER" is also hereby incorporated by reference.

Field of the Invention:

This invention relates to the field of radio frequency (RF) mixers. More particularly, this invention relates to dual balanced RF mixers with a single ended input.

Background of the Invention:

Mixer circuits are well known in the electronics industry. Mixers have many applications and their use has been extensive. One of the more common applications has been in radio frequency receivers as frequency multipliers or converters. Typically in these types of applications, an incoming modulated RF signal is combined with the signal of a local oscillator (LO) to produce a modulated intermediate frequency (IF) signal. The IF output of the mixer is the difference and sum of the frequencies between the RF and LO frequencies and is then further processed by other known circuits or devices, such as an on-chip active filter.

Many types of mixers are known. One example of a mixer commonly known in the art is the double balanced mixer or the 'Gilbert Cell' or 'Gilbert Mixer' as shown in Figure 1. The Gilbert cell is named after its inventor and since then many other mixer topologies have utilized this basic approach. Further modifications and enhancements to the Gilbert cell have been made and are known in the art as will be discussed hereinafter.

The conventional Gilbert cell mixer 10 of Figure 1 is made up of a RF input stage 20 and a mixer core 30. The RF input stage includes two transistors Q1 and Q2. The base terminal of the

first transistor Q1 is coupled to one of two RF signal inputs. The emitter terminal of the first transistor Q1 is coupled to the emitter terminal of the second transistor Q2 and to the current source I1. The collector terminal of the first transistor Q1 is connected to the first pair of differentially connected transistors Q3 and Q4 in the mixer core. The base terminal of the second transistor Q2 is coupled to the second RF signal input. The collector of the second transistor Q2 is coupled to the second pair of differentially connected transistors Q5 and Q6 in the mixer core.

The mixer core is made up of four transistors Q3, Q4, Q5, Q6 coupled as two differentially cross-coupled pairs. The first differentially cross-coupled pair Q3 and Q4 is commonly connected by way of the emitter terminals and further connected to the collector of the first transistor Q1 in the RF input stage. The second differentially cross-coupled pair Q5 and Q6 is also connected by common emitters and further coupled to the collector of the second transistor Q2 in the RF input stage. The base terminal of the first transistor Q3 in the first differential cross-coupled pair of transistors is coupled to the base terminal of the second transistor Q6 of the second differential cross-coupled pair and further coupled to one of two LO input terminals. Similarly, the base terminal of the second transistor Q4 of the first differential cross-coupled pair is coupled to the base terminal of the first transistor Q5 of the second differential cross-coupled pair and further coupled to the second LO input terminal. The collector terminal of the first transistor Q3 of the first differential cross-coupled pair is coupled to the collector terminal of the first transistor Q5 of the second differential cross-coupled pair and further connected to one of two IF output terminals. The collector terminal of the second transistor Q4 of the first differential cross-coupled pair is coupled to the collector terminal of the second transistor Q6 of the second differential cross-coupled pair and further connected to the second IF output terminal.

The operation of the Gilbert cell mixer is well known and need not be elaborated here. In spite of the advantages of the Gilbert cell, there are inherent limitations. For example, the Gilbert cell has limited dynamic range, which is the difference between IP3 (third order intercept point) and noise figure for a given power consumption. The Gilbert mixer's noise figure, linearity, and current drain performance also have been conventionally defined. Consequently, inventions since the introduction of the Gilbert cell have centered on improving various parametric

concerns usually dependent on unique mixer applications. One such case is the 'Micromixer' which is described in detail in "The MICROMIXER: A Highly Linear Variant of the Gilbert Mixer Using a Bisymmetric Class-AB Input Stage," by Barrie Gilbert, IEEE Journal of Solid-State Circuits, Vol. 32, No.9, September 1997 and hereby incorporated by reference.

Referring to Figure 2, the difference between the Micromixer and the Gilbert mixer of Figure 1 is apparent. The differential pair in the RF Input section of the Gilbert cell of Figure 1 has been replaced by a bisymmetric Class AB topology in the Micromixer of Figure 2. The operation of the Micromixer is also known in the art. This improvement over the Gilbert mixer results in increased mixer performance by way of increased linearity, accurate input impedance, high intermodulation intercepts and nearly unlimited signal capacity. It does not, however, significantly improve noise figure.

Another technique to improve the performance of conventional Gilbert mixers is the use emitter degeneration resistors. This technique, however, introduces resistive thermal noise, which degrades the dynamic range of the differential pair in the RF input section. Yet another technique to improve the performance of the Gilbert mixer involves the use of multi-tanh doublets or triplets as demonstrated in U. S. Patent Number 6,054,889, "Mixer with Improved Linear Range." While the use of multi-tanh doublet or triplet approach into a conventional Gilbert mixer improves its performance, it does so at the expense of increasing complexity and loss of valuable chip real estate. Additionally, matching impedance to 50 Ω typically requires impedance transformation at the input.

In other types of mixers, the diode ring and Schottky diode ring mixer for example, the use of baluns, active or passive, increase mixer performance. As demonstrated in U. S. Patent numbers 6,094,570, "Double-balanced Monolithic Microwave Integrated Circuit Mixer" and 6,078,802, "High Linearity Active Balance Mixer, the use of baluns is known in the art and provide the transfer of RF energy from an unbalanced structure to a balanced structure thereby increasing mixer parametric performance such as linearity and impedance matching for example. Despite advances in integrated circuit fabrication, the use of baluns still take up valuable chip real estate and their use is a compromise in circuit design.

What is needed is a mixer circuit that addresses the known deficiencies in the prior art mixers. Specifically, what is needed is an improved mixer circuit, which provides increased mixer performance by way of a single ended input, and which exhibits a high dynamic range, a low noise figure, and with no off chip differential RF circuit or baluns required.

Summary of the Invention:

Briefly, according to the invention, a mixer circuit having a single ended input and a dual output is provided. The mixer circuit is a singled ended input to a double balanced high dynamic range mixer with only two base-emitter junctions across the supply. It provides for the use of bondwires to off chip ground as DC block and DC feed elements. The single ended input and differential output balanced mixer is well suited for the input stage of an integrated radio receiver - off chip circuitry is usually single ended, but on chip circuits are usually differential. No off chip differential RF circuits or baluns are required which reduces off chip component count and improves radio performance. The mixer circuit has lower LO drive requirements because of the DC coupled LO port. This results in better radio performance and a smaller die area because of the DC coupled IF port.

The combination of all embodiments described results in a mixer performance significantly higher than the well known Gilbert Cell mixer, and whose RF, LO and IF ports require no extra on chip or off chip interface circuits. The first implementation is for 900 MHz operation in the IRIS 900 low IF receiver section. As a regular down conversion mixer (Figure 3) it achieves a noise figure of 5.5 dB, a power gain of 9 dB, an input IP3 of -8 dBm, and an input P1dB of -16dBm. Because of the impedance change from 50 ohms matched at the input to 1K + 1K differential open circuit at the output, the voltage gain is 28 dB. Power consumption is 7 mA from a 2.9 V supply. Used as a quadrature image rejection mixer the noise figure is 8.5 dB with the same gain and large signal performance.

Brief Description of the Drawings:

Figure 1 is a schematic drawing of a prior art Gilbert Cell mixer.

Figure 2 is a schematic drawing of a prior art MICROMIXER balanced mixer.

Figure 3 is a schematic drawing of a basic mixer according to the invention.

Figure 4 is a schematic drawing of a quadrature mixer according to the present invention.

Figure 5 is a schematic drawing of a mixer with a cascode connection of Q1 with RF feedback.

Figure 6 is a schematic drawing of a tracking supply for LO buffers.

Figure 7 is a schematic drawing of a tracking mixer bias current circuit.

Detailed Description of a Preferred Embodiment:

This novel mixer topology circuit was developed as the input stage of the highly integrated receiver. This application requires a down conversion mixer with a higher dynamic range than the standard Gilbert cell, and with a single ended input to interface to an off chip filter. The mixer input is at 902-928 MHz, and its output is at the 1.024 MHz intermediate frequency of the receiver.

Figure 3 shows the basic features of the new invention. The mixer 40 is generally shown. The mixer includes of the mixer core 50 and the RF input stage 60. The mixer core 50 is coupled to the RF input stage 60. The mixer core 50 includes of four transistors Q4-Q7 coupled as two differentially cross-coupled pairs as in the prior art of Figure 2. The first differential transistor pair Q4 and Q5 are common emitter connected to the RF input stage 60 by way of the collector terminal of a transistor Q2 in the RF input stage 60. Similarly, the second differential transistor pair Q6 and Q7 are also common emitter coupled to the RF input stage 60 by way of the collector terminal of transistor Q3 in the RF input stage 60.

The base terminal of the first transistor Q4 in the first differential pair of transistors is coupled to the base terminal of the second transistor Q7 of the second differential pair and further coupled to one of two LO input terminals. Similarly, the base terminal of the second transistor Q5 of the first differential pair is coupled to the base terminal of the first transistor Q6 of the second differential pair and further coupled to the second LO input terminal. The collector terminal of the first transistor Q4 of the first differential pair is coupled to the collector terminal of the first transistor Q6 of the second differential pair and further connected to one of two IF output terminals and to the first terminal of a load resistor R2. The second terminal of the

load resistor R2 is coupled to a voltage source V_{cc}. The collector terminal of the second transistor Q5 of the first differential pair is coupled to the collector terminal of the second transistor Q7 of the second differential pair and further connected to the second IF output terminal and to a second load resistor R3. The second terminal of the second load resistor R3 is also connected to the voltage source V_{cc}.

Referring to the RF input stage 60, the RF input signal is applied to the base of a first transistor Q1 via a matching network. Here, an inductor L3 is used as a matching network, however it is understood that other types of matching networks could be used. The first transistor Q1 has three principle functions:

1. It presents a reasonable input impedance (e.g. only one external inductor is required to match the input to 50 ohms);
2. It acts as phase splitter, producing out of phase waveforms at its collector and emitter.
3. It acts as a low noise input device, defining the noise figure of the mixer.

The base terminal of the first transistor Q1 is coupled to one terminal of an inductor L3 and to a biasing resistor R_{b1}. The second terminal of the inductor L3 is coupled to the RF input. The second terminal of the resistor R_{b1} is coupled to a bias current source Bias 1. The emitter terminal of the first transistor Q1 is coupled to the first terminal of an inductor L1 and further coupled to the emitter of a cascode transistor Q3. The second terminal of the inductor L3 is coupled to ground. The collector terminal of the first transistor Q1 is coupled to the first terminal of a resistor R1 and to the first terminal of a capacitor C3. The second terminal of the resistor R1 is coupled to a voltage source V_{cc} for example. The second terminal of the capacitor C3 is coupled to the first terminal of the inductor L2 and to the emitter terminal of a cascode transistor Q2.

The RF input stage 60 further includes two cascode transistors Q2 and Q3 having a common base connection. The emitter terminal of the first cascode transistor Q2 is coupled to the collector of the first transistor Q1 by way of the connections to the capacitor C3 and the

resistor R1. The emitter terminal of the second cascode transistor Q3 is coupled to the emitter terminal of the first transistor Q1 and to the first terminal of the inductor L1. The emitter terminals of the cascode transistors Q2 and Q3 are further coupled to two capacitors C1 and C2 in series and further coupled to a bias source, Bias 2.

In operation, the two cascode transistors Q2 and Q3 isolate the RF input stage 60 circuitry from the mixer core's LO drive signal and its harmonics. The mixer core's differentially coupled transistors Q4, Q5, Q6, and Q7 perform the frequency conversion from RF to IF. They act as an analog multiplier, so that the output current from the four transistors Q4, Q5, Q6, and Q7 is the product of the RF input and the LO signals. These currents develop a differential output voltage across the load resistors R2 and R3.

The cascode arrangement of the two cascode transistors Q2 and Q3 is 'folded' to increase the headroom available at the output. The emitter of the first transistor Q1 can be directly connected to the emitter of the second cascode transistor Q3, and the capacitor C3 level shifts the signal between the collector of the first transistor Q1 and the emitter of the first cascode transistor Q2.

The two inductors L1 and L2 in combination with the capacitors form a tuned circuit and provide a DC feed path, keeping the emitters of the two cascode transistor Q2 and Q3 at the same DC potential. The inductors L1, L2, and part of the input matching inductor L3 can be IC package inductances so on chip inductors are not required. The capacitors C1 and C2 tune out the inductance of the two inductors L1 and L2, and provide an RF 'center' tap' to define the RF voltage at the bases of the two cascode transistors Q2 and Q3.

In further embodiments of the invention, different transistors could be used. For example, the circuits presented could be undertaken with NPN transistors, PNP transistors, MOSFET or MESFET devices or any combination thereof using conventional design techniques for such substitutions.

Quadrature Mixer

In another embodiment of the invention, a quadrature mixer is presented. Quadrature mixers are used in image rejection, Low IF or Zero IF applications. To form the quadrature

mixer circuit of this embodiment, the mixer core 20 of Figure 3 (Q4-Q7) can be duplicated and the RF input stage 60 of Figure 3 can be modified to provide two sets of cascode transistors as is shown in Figure 4.

The quadrature mixer 70 of Figure 4, thus, is made up of a mixer core 80 and a RF input stage 90. The mixer core 80 consists of two sets of four transistors Q4-Q7 and Q10-Q13 coupled as four differentially cross-coupled transistor pairs. The first set of differentially cross coupled transistors pairs Q4-Q7 in the mixer core 70 is identical to the transistors in the mixer core of Figure 3.

Referring to Figure 4 and the first set of differentially cross-coupled transistors pairs Q4-Q7, the base terminal of the first transistor Q4 in the first differential pair of transistors Q4, Q5 is coupled to the base terminal of the second transistor Q7 of the second differential pair Q6, Q7 and further coupled to one of two In-Phase LO input terminals. Similarly, the base terminal of the second transistor Q5 of the first differential pair Q4, Q5 is coupled to the base terminal of the first transistor Q6 of the second differential pair Q6, Q7 and further coupled to the second In-Phase LO input terminal. The collector terminal of the first transistor Q4 of the first differential pair Q4, Q5 is coupled to the collector terminal of the first transistor Q6 of the second differential pair Q6, Q7 and further coupled to one of two In-Phase IF output terminals and to the first terminal of a load resistor R2. The second terminal of the load resistor R2 is coupled to a voltage source V_{cc}. The collector terminal of the second transistor Q5 of the first differential pair Q4, Q5 is coupled to the collector terminal of the second transistor Q7 of the second differential pair Q6, Q7 and further connected to the second In-Phase IF output terminal and to a first terminal of a second load resistor R3. The second terminal of the second load resistor R3 is also coupled to the voltage source V_{cc}.

The first differential transistor pair Q4, Q5 of the first set of differentially cross coupled transistors pairs Q4-Q7, are common emitter connected to the RF input stage 90 and further connected to the collector terminal of a transistor Q2 in the RF input stage 90. Similarly, the second differential transistor pair Q6, Q7 are also common emitter connected to the RF input stage 90 by way of the collector terminal of a transistor Q3 in the RF input stage 90.

Referring again to Figure 4 and now the second set of differentially cross coupled transistors pairs Q10-Q13, the base terminal of the first transistor Q10 in the first differential pair of transistors Q10, Q11 is coupled to the base terminal of the second transistor Q13 of the second differential pair Q12, Q13 and further coupled to one of two Quadrature Phase LO input terminals. Similarly, the base terminal of the second transistor Q11 of the first differential pair of transistors Q10, Q11 is coupled to the base terminal of the first transistor Q12 of the second differential pair of transistors Q12, Q13 and further coupled to the second Quadrature Phase LO input terminal. The collector terminal of the first transistor Q10 of the first differential pair of transistors Q10, Q11 is coupled to the collector terminal of the first transistor Q12 of the second differential pair of transistors Q12, Q13 and further coupled to one of two Quadrature Phase IF output terminals and to the first terminal of a load resistor R4. The second terminal of the load resistor R4 is coupled to a voltage source V_{cc}. The collector terminal of the second transistor Q11 of the first differential pair of transistors Q10, Q11 is coupled to the collector terminal of the second transistor Q13 of the second differential pair of transistors Q12, Q13 and further coupled to the second Quadrature Phase IF output terminal and to a first terminal of a second load resistor R5. The second terminal of the second load resistor R5 is also coupled to the voltage source V_{cc}.

The first differential transistor pair Q10, Q11 of the second set of differentially cross coupled transistors pairs Q10-Q13, have their common emitters connected to the RF input stage 90 by way of the collector terminal of a transistor Q8 in the RF input stage 90. Similarly, the second differential transistor pair Q12, Q13 are also common emitter coupled to the RF input stage 90 by way of the collector terminal of a transistor Q9 in the RF input stage 90.

Referring now to the RF input stage 90 of Figure 4, the base terminal of the input transistor, Q1, is coupled to one terminal of a biasing resistor, R_{b1} and to an inductor, L3. The second terminal of the inductor L3 is coupled to the RF signal input. The second terminal of the biasing resistor R_{b1} is coupled to a bias current source Bias 1. The emitter terminal of the input transistor Q1 is coupled to the first terminal of an inductor L1 and further coupled to the emitter terminals of two cascode transistors Q3, Q9. The second terminal of the inductor L3 is coupled to ground. The collector terminal of the input transistor Q1 is coupled to the first terminal of a

resistor R1 and to the first terminal of a capacitor C3. The second terminal of the resistor R1 is coupled to a voltage source V_{cc} for example. The second terminal of the capacitor C3 is coupled to the first terminal of the inductor L2 and to the emitter terminals of two cascode transistors Q2, Q8.

The RF input stage 90 includes two pairs of cascode transistors Q2, Q3 and Q8, Q9. The first pair of cascode transistors Q2, Q3 has a common base connection and is further coupled to two capacitors C1, C2 and to the first terminal of a biasing resistor R_{b2}. The emitter terminal of the first cascode transistor Q2 of the first pair of cascode transistors Q2, Q3 is coupled to the collector terminal of the input transistor Q1 by way of the connections to the capacitor C3 and the inductor L2. The emitter terminal of the second cascode transistor Q3 of the first pair of cascode transistors Q2, Q3 is coupled to the emitter terminal of the input transistor Q1 and the emitter terminal of the second cascode transistor Q9 of the second pair of cascode transistors Q8, Q9, and to the first terminal of the inductor L1. The emitter terminals of the first pair of cascode transistors Q2, Q3 are further conupled to two capacitors C1 and C2 in series and further coupled to a bias source, Bias 2 by way of a biasing resistor R_{b2}.

The second pair of cascode transistors Q8, Q9 also have a common base connection. The base terminals of the second pair of cascode transistors Q8, Q9 are further coupled to the first terminal of a biasing resistor R_{b3} and to two capacitors C4, C5. The emitter terminal of the first cascode transistor Q8 of the second pair of cascode transistors Q8, Q9 is coupled the emitter terminal of the input transistor Q1 and to the first cascode transistor Q2 of the first pair of cascode transistors Q1, Q2. The emitter terminal of the second cascode transistor Q9 of the second pair of cascode transistors Q8, Q9 is coupled the input transistor Q1 and to the second cascode transistor Q3 of the first pair of cascode transistors Q2, Q3. The second terminal of the biasing resistor R_{b2} is coupled to the second terminal of the biasing resistor R_{b3} and further coupled to a bias source Bias 2.

In operation the quadrature mixer operates similarly to other quadrature mixers. The output current from the input transistor is split between the two sets of cascode transistors. If a quadrature pair of LO drive signals is provided to the LO ports, then a quadrature IF output is available at the two IF ports. The LO input signals in the quadrature mixer are the in-phase

portion and the quadrature phase portion of the LO drive signal. The IF output signals are the in-phase portion and the quadrature phase portion of the IF output signal.

RF Feedback

Referring to Figure 5, another embodiment is presented to improve the phase splitting capacity of the input transistor and thereby improve the overall mixer performance. The single input transistor Q1 does not give a perfect 180-degree phase split between its collector and emitter terminals. Some of this is caused by the differing impedances at the collector and base - the impedance at the emitter terminal of a second cascode transistor Q3 is half that at the emitter terminal of a first cascode transistor Q2. Another cause of error is the capacitive feedback through the base-collector capacitance of the single input transistor Q1. To improve the phase balance and accurately define the gain, the single input transistor Q1 can be replaced with a cascode connection of two transistors and a resistive feedback added to define the forward gain.

The mixer circuit of Figure 5 is identical to the mixer circuit of Figure 3 with the exception of the an added cascode transistor Q8 coupled to the input transistor Q1 and the added resistive feedback circuit including of a capacitor C4 coupled in series to a resistor R4. Referring to Figure 5, the collector terminal of the input transistor Q1 is coupled to the emitter terminal of the cascode transistor Q8. The base terminal of the cascode transistor Q8 is coupled to a voltage source Vcc. The collector terminal of the cascode transistor Q8 is coupled to the first terminal of a resistor R1 and to the first terminal of a capacitor C3, which is similar to the connection of the input transistor Q1 in Figure 3 and further coupled to a first terminal of another capacitor C4. The second terminal of the capacitor C4 is coupled to the first terminal of a resistor R4. The second terminal of the resistor R4 is coupled to the base terminal of the input transistor Q1.

LO Port Biasing

To obtain the maximum dynamic range from these mixers, enough voltage headroom must be preserved at the collectors terminals of the differentially cross coupled transistors Q4-Q7 that the full output signal can be developed across the load resistors R2 and R3. At the same time, to stabilize the gain of the mixer it is desirable to keep the transconductances of the

transistors constant with temperature. This requires that the bias current be proportional to absolute temperature (PTAT). If the LO inputs are driven by a Common Mode Logic (CML) buffer with emitter follower outputs (common collector amplifiers), then the common mode DC voltage at the LO inputs will be at V_{CC} - V_{be}, and will rise with temperature. The voltage drop across the load resistors R2, R3 will increase with temperature because of the PTAT biasing. The combined effect is to reduce the V_{CE} of the differentially cross-coupled transistors Q4-Q7 at high temperatures, leading to saturation. Reducing the load resistors R2, R3 to avoid saturation at high temperature results in a loss of gain, and poor use of available supply voltage.

The solution employed is to power the LO buffers from a tracking supply. The supply generates $3* V_{be} + 0.2$ V. This keeps the V_{cb} of the cascode devices (Q2 and Q3) constant at around 0 V. The total headroom at the load resistors R2, R3 is from $V_{bc} + V_{cesat} + 0.2$ to V_{cc}. This headroom increases with temperature to allow for the PTAT current bias.

Referring to Figure 6, one implementation of a tracking supply is shown. It is a conventional low dropout voltage regulator, except that the reference voltage is $2 * V_{be} + 133$ mV. The amplifier has a closed loop gain of 1.5, so that the output voltage of the regulator is $3 * V_{be} + 0.2$ V. Figure 6 shows a single CML buffer with emitter followers. The common mode voltage at the output of the followers will be at $+2 * V_{be}$, and remain there over process and temperature variations.

The tracking supply of Figure 6 includes a first diode-connected transistor Q1 in series with a second diode-connected transistor Q2 and a resistor R1 in series with the second diode-connected transistor Q2. The cathode of the first diode-connected transistor Q1 is coupled to ground and the anode is coupled to the cathode of the second diode-connected transistor Q2. The anode of the second diode-connected transistor Q2 is coupled to the first terminal of a resistor R1. The second terminal of the resistor R1 is coupled to a current source, which is coupled to the voltage source V_{CC}.

The tracking supply circuit further includes an amplifier and a CML buffer. The amplifier includes four terminals. The first terminal of the amplifier is coupled to the second terminal of the resistor R1 and to a current source. The second terminal of the amplifier is

coupled to the voltage supply V_{cc}. The third terminal of the amplifier is coupled to ground and the fourth terminal is coupled to the CML buffer.

The CML buffer includes two common emitter coupled transistors Q3, Q4. The emitter terminals of the two common emitter transistors Q3, Q4 are coupled together and further coupled to ground by way of a connection to a current supply. The base terminal of the first transistor Q3 is coupled to one of two LO drive inputs. The collector terminal of the first transistor Q3 is coupled to the base of one of two common collector amplifiers Q6 and to a first terminal of a resistor R2. The base terminal of the second transistor Q4 is coupled to the second LO drive input. The collector terminal of the second transistor Q4 is coupled to the base terminal of the second common collector amplifier Q5 and to a first terminal of a resistor R3. The emitter of the first common collector amplifier Q5 is coupled to one of two mixer LO drive input terminals and to ground by way of a current source. The collector terminal of the first common collector amplifier Q5 is coupled to the collector terminal of the second common collector amplifier Q6 and to the fourth terminal of the amplifier by way of connections to the second terminals of the first and second resistors R2, R3. The emitter of the second common collector amplifier Q6 is coupled to the second mixer LO drive input terminal and to ground by way of a current source.

Output Common Mode Voltage Control

The output of the mixer is buffered by emitter followers then feeds an on chip active filter for channel selectivity. Ideally the output of the mixer should be DC coupled to the filter. This requires that the common mode voltage at the mixer output match up with the common mode input range of the filter. The tracking bias circuit shown in Figure 7 does this with a fairly simple replica bias generator.

Referring to Figure 7, the tracking bias circuit consists of a first transistor Q1 coupled as a diode-connected transistor having an anode coupled to the first terminal a first resistor R1 and the cathode coupled to the collector terminal of a second transistor Q2. The second terminal of the resistor R1 is coupled to a voltage source V_{cc}. The emitter terminal of the second transistor Q2 is coupled to ground. The base terminal of the second transistor Q2 is coupled to the first

terminal of a second resistor R2. The second terminal of the second resistor R2 is coupled to the output terminal of a loop amplifier and to the bias current terminal Bias 2 of the mixer.

The tracking bias circuit further includes a loop amplifier. The loop amplifier Q3 includes three terminals. The first terminal of the loop amplifier is coupled to the cathode terminal of the diode-connected transistor Q1. The second terminal of the loop amplifier is coupled to the first terminal of a bandgap voltage supply V_{bg}. The third terminal of the loop amplifier is coupled to the second terminal of the second resistor R2 and further coupled to the bias current terminal Bias 2 of the mixer. The second terminal of the bandgap voltage supply is coupled to ground.

In operation, the filter that follows the mixers has its input common mode range centered on the chip bandgap reference voltage ($V_{bg} \sim 1.25$ V). The desired output common mode voltage of the mixers is therefore $V_{bg} + V_{be}$. The simple circuit in Figure 7 achieves this. R1, Q1 and Q2 are ratioed to the corresponding components in the mixer (R2 & R3, Q4 to Q7 and Q2 to Q3) so that they operate at the same current density. The loop amplifier compares the voltage at the first transistor Q1 emitter terminal (a replica of the mixer output common mode voltage) with the bandgap voltage (the desired common mode voltage). With the appropriate feedback, the mixer output common mode voltage is held at the bandgap voltage.

In the application with the mixer operating at a 2.9 V supply, this circuit also generates a partially PTAT bias current. The voltage across the mixer load resistors is $V_{cc} - V_{be} - V_{bg}$. With $V_{cc} - V_{bg} = 1.65$ V the current in R1 is half PTAT. This partially compensates the temperature variation of the device transconductance.

The present invention has been described in terms of specific embodiments incorporating details to facilitate the understanding of the principles of construction and operation of the invention. Such references herein to specific embodiments and details thereof are not intended to limit the scope of the claims appended hereto. It will be apparent to those skilled in the art that modifications may be made in the embodiments chosen for illustration without departing from the spirit and scope of the invention. Specifically, it will be apparent to one of ordinary skill in the art that the circuits of the present invention could be implemented in several different

ways and the circuits disclosed above are only illustrative of the preferred embodiments of the invention and are in no way limitations.

Claims

What is claimed is:

1. A mixer circuit for generating an IF output responsive to an RF input and a LO drive source, comprising:

a mixer core having a doubly balanced mixer including a first differentially coupled transistor pair and a second differentially coupled transistor pair;

an RF input circuit coupled to the mixer core, the RF input circuit comprising:

an input inductor having a first terminal coupled to receive an RF input signal and a second terminal;

a biasing resistor having a first terminal coupled to the second terminal of the input inductor and a second terminal coupled to a first bias voltage;

a first input transistor having a control terminal coupled to the second terminal of the input inductor, a second terminal, and a third terminal;

a second inductor having a first terminal coupled to the second terminal of the first input transistor and to the first differentially coupled transistor pair, the second inductor also having a second terminal coupled to a ground potential;

a supply resistor having a first terminal coupled to the second terminal of the first input transistor and a second terminal coupled to a supply potential;

a first capacitor having a first terminal also coupled to the second terminal of the first input transistor and a second terminal coupled to the second differentially coupled transistor pair; and

a third inductor having a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the ground potential.

2. The mixer circuit according to Claim 1 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all npn transistors.

3. The mixer circuit according to Claim 1 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all pnp transistors.

4. The mixer circuit according to Claim 1 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all MOSFET transistors.

5. The mixer circuit according to Claim 1 wherein the first differentially coupled transistor pair, the second differentially coupled transistor pair and the first input transistor are all MESFET transistors.

6. A mixer circuit for generating an IF output responsive to an RF input and a LO drive source, comprising:

a mixer core having a doubly balanced mixer including a first differentially coupled npn transistor pair and a second differentially coupled npn transistor pair, the mixer core coupled to receive a LO drive signal, the LO drive signal having a plurality of harmonics;

a low noise RF input circuit coupled to the mixer core through a cascode circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the cascode circuit further isolates the RF input circuit from the LO drive signal and the plurality of harmonics.

7. A mixer as in Claim 6 wherein the cascode circuit comprises:

a first cascode transistor having an emitter terminal coupled to the second terminal of the first capacitor and to the first terminal of the third inductor, a collector terminal coupled to the second differentially coupled npn transistor pair and a base terminal,

a second cascode transistor having a base terminal coupled to the base terminal of the first cascode transistor, an emitter terminal coupled to the first terminal of the second inductor and to the emitter terminal of the first npn transistor and a collector terminal coupled to the first differentially coupled npn transistor pair,

a second capacitor, having a first terminal coupled to the collector terminal of the first cascode transistor and a second terminal coupled to the base terminal of the first cascode transistor and to the base terminal of the second cascode transistor,

a third capacitor, having a first terminal coupled to the emitter terminal of the second cascode transistor and a second terminal coupled to the second terminal of the second capacitor and to the base terminal of the first cascode transistor and to the base terminal of the first cascode transistor,

a second biasing resistor having a first terminal coupled to the second terminal of the third capacitor and a second terminal coupled to a second bias voltage.

8. A mixer as in Claim 7, wherein the low noise RF input circuit further includes a RF feedback circuit, the RF feedback circuit comprising:

a second npn transistor having a base terminal coupled to the supply potential, an emitter terminal coupled to the collector terminal of the first input npn transistor and a collector terminal coupled to the first terminal of the supply resistor and to the first terminal of the first capacitor,

a feedback resistor, having a first terminal coupled to the base terminal of the first input npn transistor and a second terminal,

a second capacitor, having a first terminal coupled to the second terminal of the feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

9. A mixer as in Claim 7, wherein the mixer core further includes a tracking supply circuit, the tracking supply circuit comprising:

a first diode-connected transistor having a cathode terminal coupled to the ground potential and an anode terminal,

a second diode-connected transistor having a cathode terminal coupled to the anode terminal of the first diode connected transistor and an anode terminal,

a third resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal,

a first current supply having a first terminal coupled to the second terminal of the third resistor and a second terminal coupled to the supply potential,

a loop amplifier having a first terminal coupled to the second terminal of the third resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal,

a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal,

a second npn transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal,

a third npn transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second npn transistor and a collector terminal,

a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third npn transistor

a second current supply having a first terminal coupled to the emitter terminal of the second npn transistor and to the emitter terminal of the third npn transistor and a second terminal coupled to the ground potential,

a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the third npn transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input,

a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential,

a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the second npn transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input,

a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential.

10. A mixer as in Claim 7, wherein the low noise RF input circuit further includes a

tracking mixer bias current circuit coupled to the second bias input terminal, the tracking mixer bias current circuit comprising:

a third resistor having a first terminal coupled to the supply potential and a second terminal,

a first diode connected transistor having a anode terminal coupled to the second terminal of the third resistor and a cathode terminal,

a second npn transistor having a collector terminal coupled to the cathode terminal of the first diode connected transistor, an emitter terminal coupled to the ground potential and a base terminal,

a loop amplifier having a first terminal coupled to the emitter terminal of the first diode connected transistor and to the collector terminal of the second npn transistor, a second terminal coupled to the second bias voltage and a third terminal,

a fourth resistor having a first terminal coupled to the base terminal of the second npn transistor and a second terminal coupled to the second terminal of the loop amplifier and to the second bias voltage,

a bandgap voltage supply having a first terminal coupled to the ground potential and a second terminal coupled to the third terminal of the loop amplifier.

11. A mixer circuit as in Claim 6, wherein the mixer core further includes a tracking supply circuit, the tracking supply circuit comprising:

a first diode-connected transistor having a cathode terminal coupled to the ground potential and an anode terminal,

a second diode-connected transistor having a cathode terminal coupled to the anode terminal of the first diode connected transistor and an anode terminal,

a third resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal,

a first current supply having a first terminal coupled to the second terminal of the third resistor and a second terminal coupled to the supply potential,

a loop amplifier having a first terminal coupled to the second terminal of the third resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal,

a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal,

a second npn transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal,

a third npn transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second npn transistor and a collector terminal,

a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third npn transistor

a second current supply having a first terminal coupled to the emitter terminal of the second npn transistor and to the emitter terminal of the third npn transistor and a second terminal coupled to the ground potential,

a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the third npn transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input,

a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential,

a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the second npn transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input,

a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential.

12. A mixer circuit as in Claim 6, wherein the low noise RF input circuit further includes a RF feedback circuit coupled to the RF input circuit, the RF feedback circuit comprising:

a second npn transistor having a base terminal coupled to the supply potential, an emitter terminal coupled to the collector terminal of the first input npn transistor and a collector terminal coupled to the first terminal of the supply resistor and to the first terminal of the first capacitor,

a feedback resistor, having a first terminal coupled to the base terminal of the first input npn transistor and a second terminal,

a second capacitor, having a first terminal coupled to the second terminal of the feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

13. A quadrature mixer circuit for generating a quadrature IF output responsive to an RF input and a quadrature pair of LO drive signals, comprising:

a mixer core having a first doubly balanced mixer including a first differentially coupled npn transistor pair and a second differentially coupled npn transistor pair and a second doubly balanced mixer including a third differentially coupled npn transistor pair and a fourth differentially coupled npn transistor pair;

an RF input circuit coupled to the mixer core, the RF input circuit comprising:

an input inductor having a first terminal coupled to receive an RF input signal and a second terminal;

a biasing resistor having a first terminal coupled to the second terminal of the input inductor and a second terminal coupled to a first bias voltage;

a first input npn transistor having a base terminal coupled to the second terminal of the input inductor, an emitter terminal, and a collector terminal;

a second inductor having a first terminal coupled to the emitter of the first npn transistor and to the first differentially coupled npn transistor pair and to the third differentially

coupled npn transistor pair, the second inductor also having a second terminal coupled to a ground potential;

a supply resistor having a first terminal coupled to the collector of the first transistor and a second terminal coupled to a supply potential;

a first capacitor having a first terminal also coupled to the collector of the first transistor and a second terminal coupled to the second differentially coupled npn transistor pair and to the fourth differentially coupled npn transistor pair; and

a third inductor having a first terminal coupled to the second terminal of the first capacitor and a second terminal coupled to the ground potential.

14. A quadrature mixer circuit for generating a quadrature IF output responsive to an RF input and a quadrature pair of LO drive signals, comprising:

a mixer core having a first doubly balanced mixer including a first differentially coupled npn transistor pair and a second differentially coupled npn transistor pair and having a second doubly balanced mixer including a third differentially coupled npn transistor pair and a fourth differentially coupled npn transistor pair; the mixer core coupled to receive a quadrature LO drive signal, the quadrature LO drive signal having a plurality of harmonics;

a low noise RF input circuit coupled to the mixer core through a cascode circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the cascode circuit further isolates the RF input circuit from the quadrature LO drive signal and the plurality of harmonics.

15. A quadrature mixer as in Claim 14 wherein the cascode circuit comprises:

a first cascode transistor having an emitter terminal coupled to the second terminal of the first capacitor and to the first terminal of the third inductor, a collector terminal coupled to the second differentially coupled npn transistor pair and a base terminal,

a second cascode transistor having a base terminal coupled to the base terminal of the first cascode transistor, an emitter terminal coupled to the first terminal of the second inductor and to the emitter terminal of the first npn transistor and a collector terminal coupled to the first differentially coupled npn transistor pair,

a second capacitor, having a first terminal coupled to the collector terminal of the first cascode transistor and a second terminal coupled to the base terminal of the first cascode transistor and to the base terminal of the second cascode transistor,

a third capacitor, having a first terminal coupled to the emitter terminal of the second cascode transistor and a second terminal coupled to the second terminal of the second capacitor and to the base terminal of the first cascode transistor and to the base terminal of the first cascode transistor,

a second biasing resistor having a first terminal coupled to the second terminal of the second capacitor and the first terminal of the third capacitor and a second terminal coupled to a second bias voltage,

a third biasing resistor having a first terminal coupled to the second bias voltage and to the second terminal of the second biasing resistor and having a second terminal,

a third cascode transistor having a collector terminal coupled to the fourth differentially coupled npn transistor pair, an emitter terminal coupled to the second terminal of the third inductor and to the emitter terminal of the first cascode transistor, and a base terminal,

a fourth cascode transistor having a base terminal coupled to the base terminal of the third cascode transistor, a collector terminal coupled the third differentially coupled npn transistor pair and an emitter terminal coupled to the emitter terminal of the second cascode transistor and to the second terminal of the second inductor,

a fourth capacitor having a first terminal coupled to the emitter terminal of the third cascode transistor and a second terminal coupled to the base terminal of the third and fourth cascode transistors,

a fifth capacitor having a first terminal coupled to the second terminal of the fourth capacitor and to the base terminals of the third and fourth cascode transistors and a second terminal coupled to the emitter terminal of the fourth cascode transistor.

16. A quadrature mixer as in Claim 15 wherein the low noise RF input circuit further includes a RF feedback circuit, the RF feedback circuit comprising:

a second npn transistor having a base terminal coupled to the supply potential, an emitter terminal coupled to the collector terminal of the first input npn transistor and a collector terminal coupled to the first terminal of the supply resistor and to the first terminal of the first capacitor,

a feedback resistor, having a first terminal coupled to the base terminal of the first input npn transistor and a second terminal,

a sixth capacitor, having a first terminal coupled to the second terminal of the feedback resistor and a second terminal coupled to the first terminal of the supply resistor.

17. A quadrature mixer as in Claim 16, wherein the mixer core further includes a first tracking supply circuit portion coupled to the In-Phase LO drive input terminals of the mixer core and a second tracking supply circuit portion coupled to the Quadrature Phase LO drive input terminals of the mixer core.

18. A mixer circuit as in Claim 17, wherein the first tracking supply comprises:

a. a first diode-connected transistor having a cathode terminal coupled to the ground potential and an anode terminal;

b. a second diode-connected transistor having a cathode terminal coupled to the anode terminal of the first diode connected transistor and an anode terminal,

c. a third resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal;

d. a first current supply having a first terminal coupled to the second terminal of the third resistor and a second terminal coupled to the supply potential;

e. a loop amplifier having a first terminal coupled to the second terminal of the third resistor and to the first terminal of the first current supply, a second terminal

coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal;

f. a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal;

g. a second npn transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal;

h. a third npn transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second npn transistor and a collector terminal;

i. a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third npn transistor;

j. a second current supply having a first terminal coupled to the emitter terminal of the second npn transistor and to the emitter terminal of the third npn transistor and a second terminal coupled to the ground potential;

k. a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the third npn transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input;

l. a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential;

m. a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the second npn transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input; and

n. a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential;

and wherein the second tracking supply circuit portion comprises:

o. a third diode-connected transistor having a cathode terminal coupled to the ground potential and an anode terminal;

p. a fourth diode-connected transistor having a cathode terminal coupled to the anode terminal of the third diode connected transistor and an anode terminal;

q. a third resistor having a first terminal coupled to the anode terminal of the second diode connected transistor and a second terminal;

r. a first current supply having a first terminal coupled to the second terminal of the third resistor and a second terminal coupled to the supply potential;

s. a loop amplifier having a first terminal coupled to the second terminal of the third resistor and to the first terminal of the first current supply, a second terminal coupled to the supply potential, a third terminal coupled to the ground potential and a fourth terminal;

t. a fourth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal;

u. a second npn transistor having a collector terminal coupled to the second terminal of the fourth resistor, a base terminal coupled to receive a first LO drive signal and emitter terminal;

v. a third npn transistor having a base terminal coupled to receive a second LO drive signal, an emitter terminal coupled to the emitter terminal of the second npn transistor and a collector terminal;

w. a fifth resistor having a first terminal coupled to the fourth terminal of the loop amplifier and a second terminal coupled to the collector terminal of the third npn transistor;

x. a second current supply having a first terminal coupled to the emitter terminal of the second npn transistor and to the emitter terminal of the third npn transistor and a second terminal coupled to the ground potential;

y. a first common collector amplifier having a base terminal coupled to the second terminal of the fifth resistor and to the collector terminal of the third npn transistor, a collector terminal coupled to the fourth terminal of the loop amplifier, and an emitter terminal coupled to a first mixer core LO input;

z. a third current supply having a first terminal coupled to the emitter terminal of the first common collector amplifier and a second terminal coupled to the ground potential;

aa. a second common collector amplifier having a base terminal coupled to the second terminal of the fourth resistor and to the collector terminal of the second npn transistor, a collector terminal coupled to the fourth terminal of the loop amplifier and an emitter terminal coupled to a second mixer core LO input;

bb. a fourth current supply having a first terminal coupled to the emitter terminal of the second common collector amplifier and a second terminal coupled to the ground potential.

19. A quadrature mixer as in Claim 15, wherein the low noise RF input circuit further includes a tracking mixer bias current circuit, the tracking bias current circuit comprising:

a first resistor having a first terminal coupled to the supply potential and a second terminal,

a first diode connected transistor having a anode terminal coupled to the second terminal of the third resistor and a cathode terminal,

a second npn transistor having a collector terminal coupled to the cathode terminal of the first diode connected transistor, an emitter terminal coupled to the ground potential and a base terminal,

a loop amplifier having a first terminal coupled to the emitter terminal of the first diode connected transistor and to the collector terminal of the second npn transistor, a second terminal coupled to the second bias voltage and a third terminal,

a second resistor having a first terminal coupled to the base terminal of the second npn transistor and a second terminal coupled to the second terminal of the loop amplifier and to the second bias voltage,

a bandgap voltage supply having a first terminal coupled to the ground potential and a second terminal coupled to the third terminal of the loop amplifier.

20. A mixer circuit for generating an IF output responsive to an RF input and a LO drive source, comprising:

a mixer core having a doubly balanced mixer including a first differentially coupled npn transistor pair and a second differentially coupled npn transistor pair;

a single ended RF input circuit coupled to receive an RF signal, the RF circuit coupled to the mixer core, the RF circuit including means for providing an input impedance, means for splitting a phase of the RF signal, and means for decoupling noise from the RF signal to the mixer core.

21. A mixer circuit for generating an IF output responsive to an RF input and a LO drive source, comprising:

a mixer core having a doubly balanced mixer including a first differentially coupled npn transistor pair and a second differentially coupled npn transistor pair, the mixer core coupled to receive a LO drive signal, the LO drive signal having a plurality of harmonics;

a low noise single ended RF input circuit coupled to the mixer core through a cascode circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the cascode circuit further isolates the RF input circuit from the LO drive signal and the plurality of harmonics the RF circuit including means for providing an input impedance and means for splitting a phase of the RF signal.

Abstract

The mixer circuit is a singled ended input to a double balanced high dynamic range mixer with only two base-emitter junctions across the supply. It provides for the use of bondwires to off chip ground as DC block and DC feed elements. The single ended input and differential output balanced mixer is well suited for the input stage of an integrated radio receiver - off chip circuitry is usually single ended, but on chip circuits are usually differential. No off chip differential RF circuits or baluns are required which reduces off chip component count and improves radio performance. The mixer circuit has lower LO drive requirements because of the DC coupled LO port. This results in better radio performance and a smaller die area because of the DC coupled IF port.

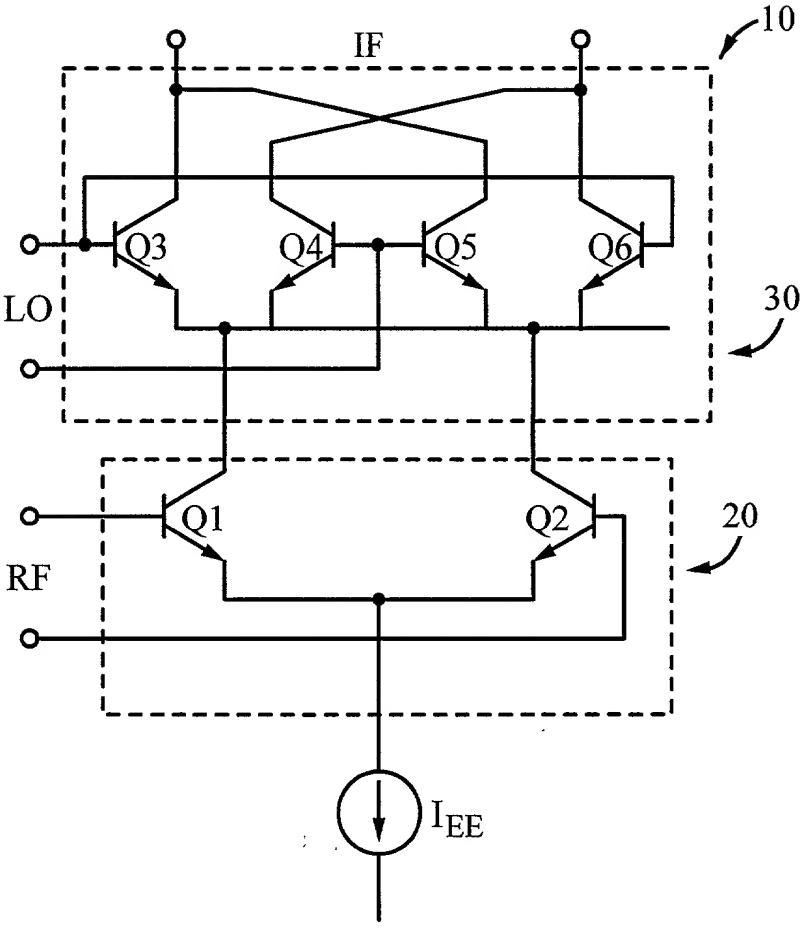


Fig. 1 PRIOR ART

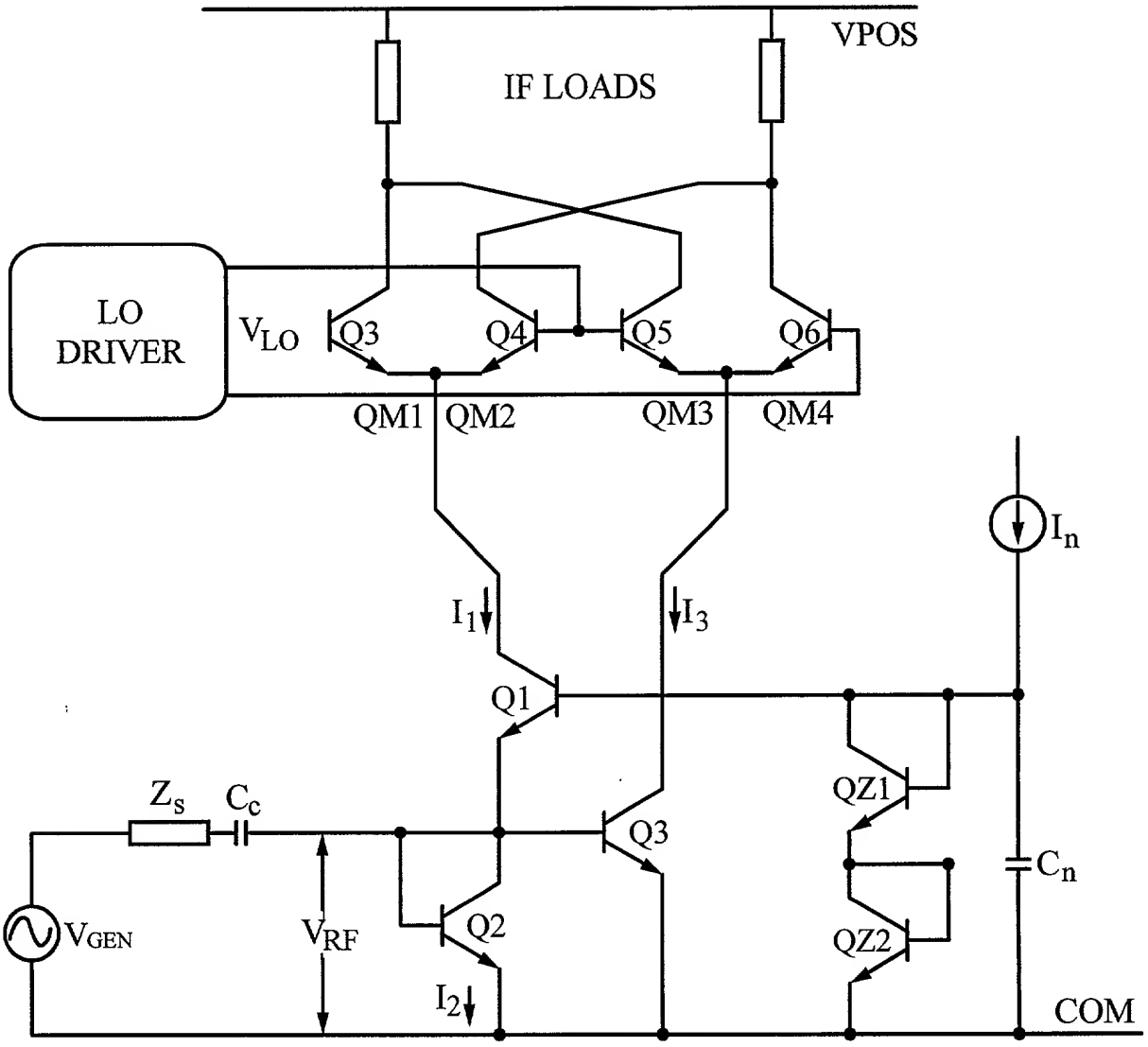
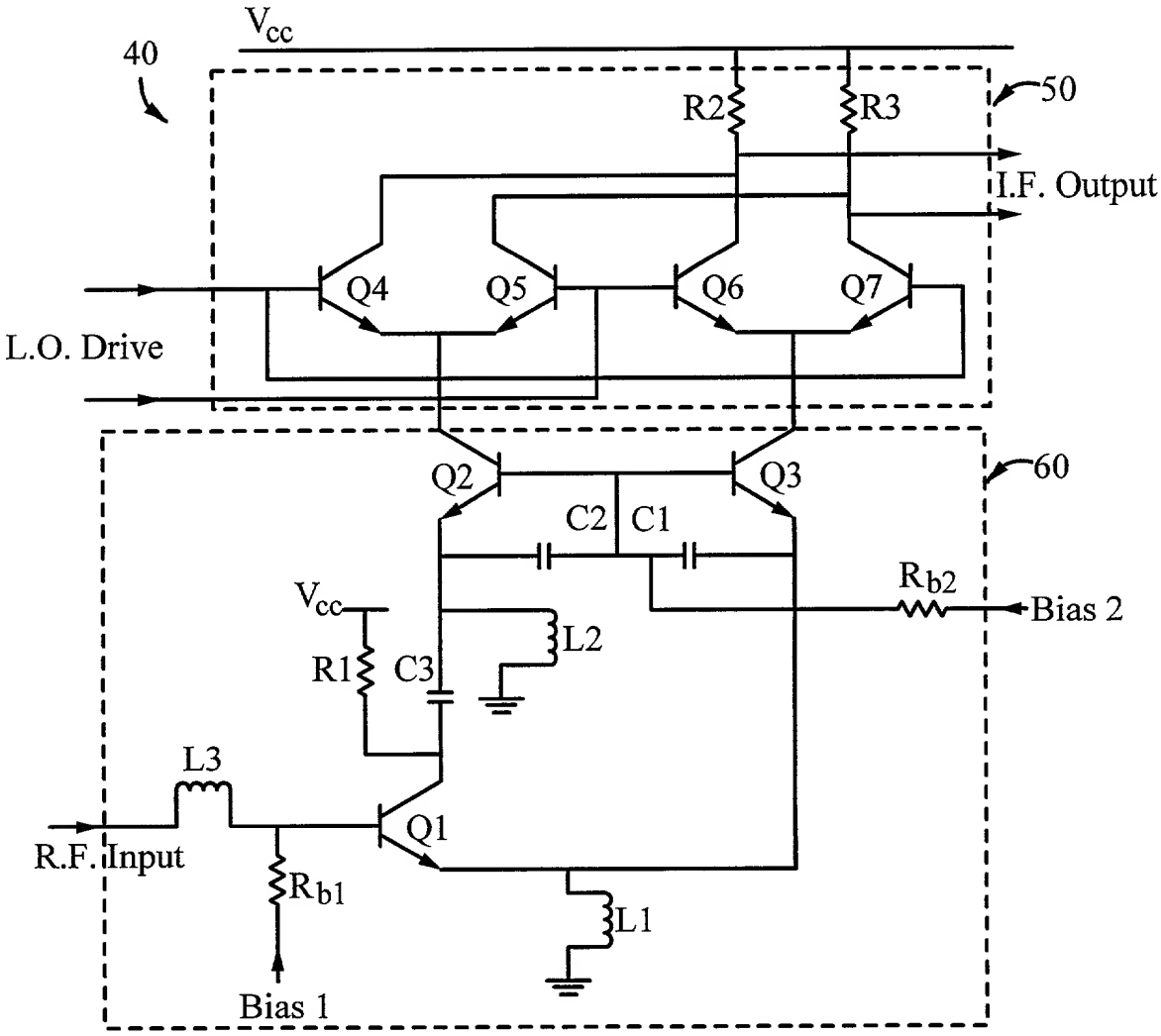


Fig. 2 PRIOR ART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50
R2
R3
I.F. Output
Q4
Q5
Q6
Q7
L.O. Drive
60
Q2
Q3
C2
C1
Rb2
Bias 2
Vcc
L2
R1
C3
L3
Q1
R.F. Input
Rb1
L1
Bias 1

Fig. 3

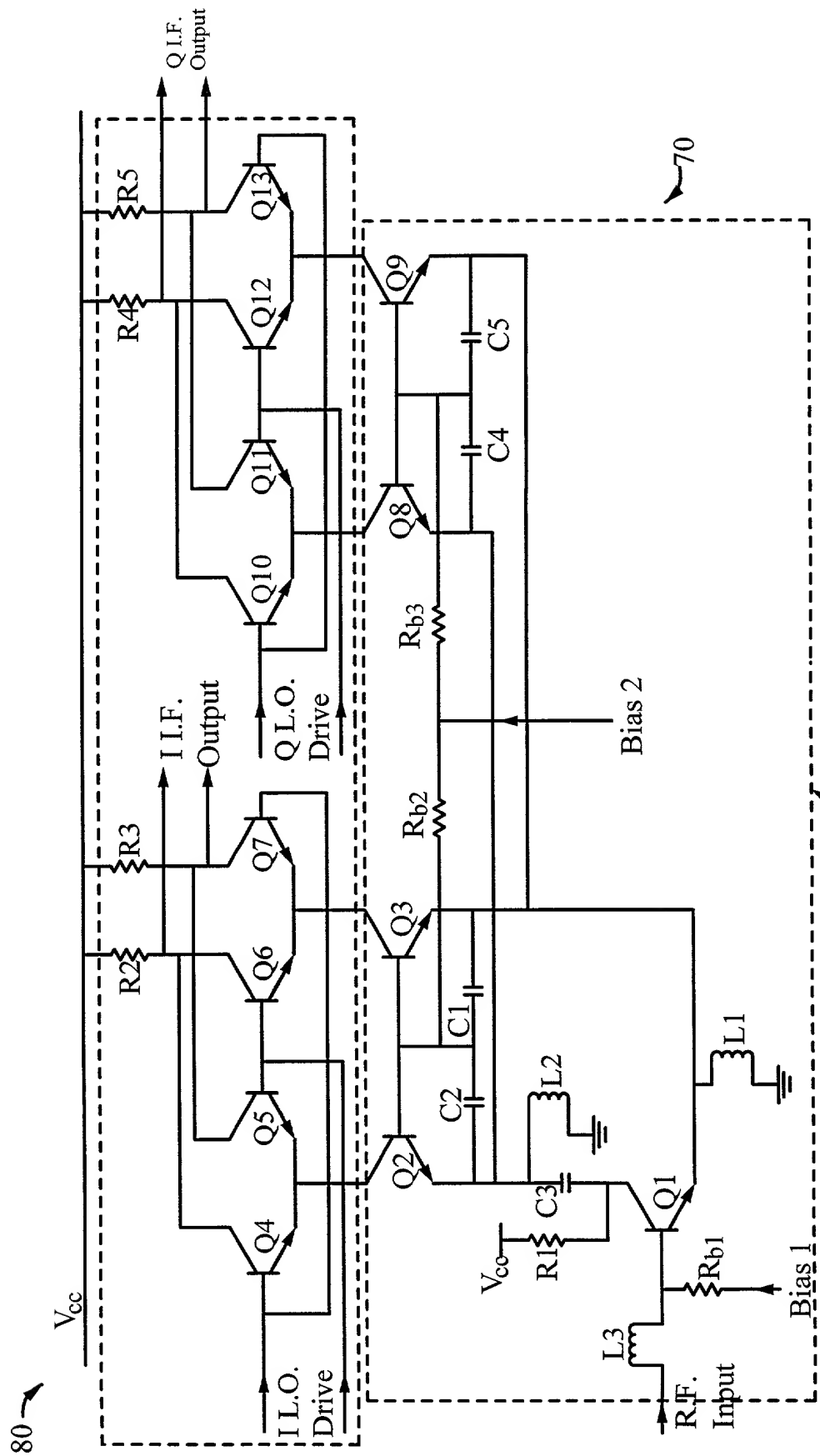
80
Vcc
I L.O. Drive
Q4
Q5
Q6
Q7
R2
R3
I I.F. Output
Q L.O. Drive
Q10
Q11
Q12
Q13
R4
R5
Q I.F. Output
Q1
Q2
Q3
Q8
Q9
C1
C2
C3
C4
C5
L1
L2
L3
Rb1
Rb2
Rb3
R1
Vcc
Bias 1
Bias 2
R.F. Input
70
90

Fig. 4

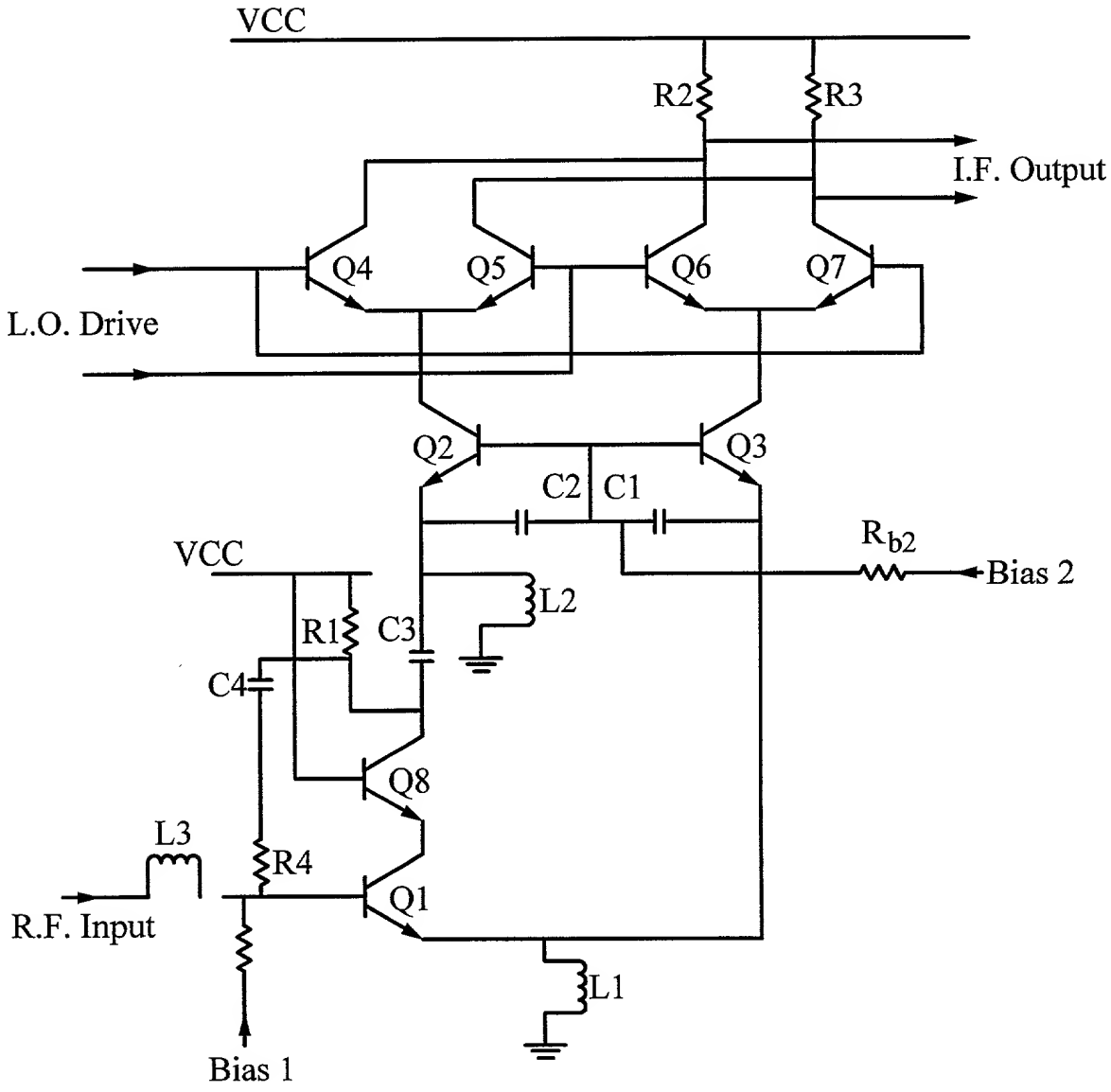
VCC
R2
R3
I.F. Output
Q4
Q5
Q6
Q7
L.O. Drive
Q2
Q3
C2
C1
VCC
R_{b2}
Bias 2
L2
R1
C3
C4
Q8
L3
R4
Q1
R.F. Input
L1
Bias 1

Fig. 5

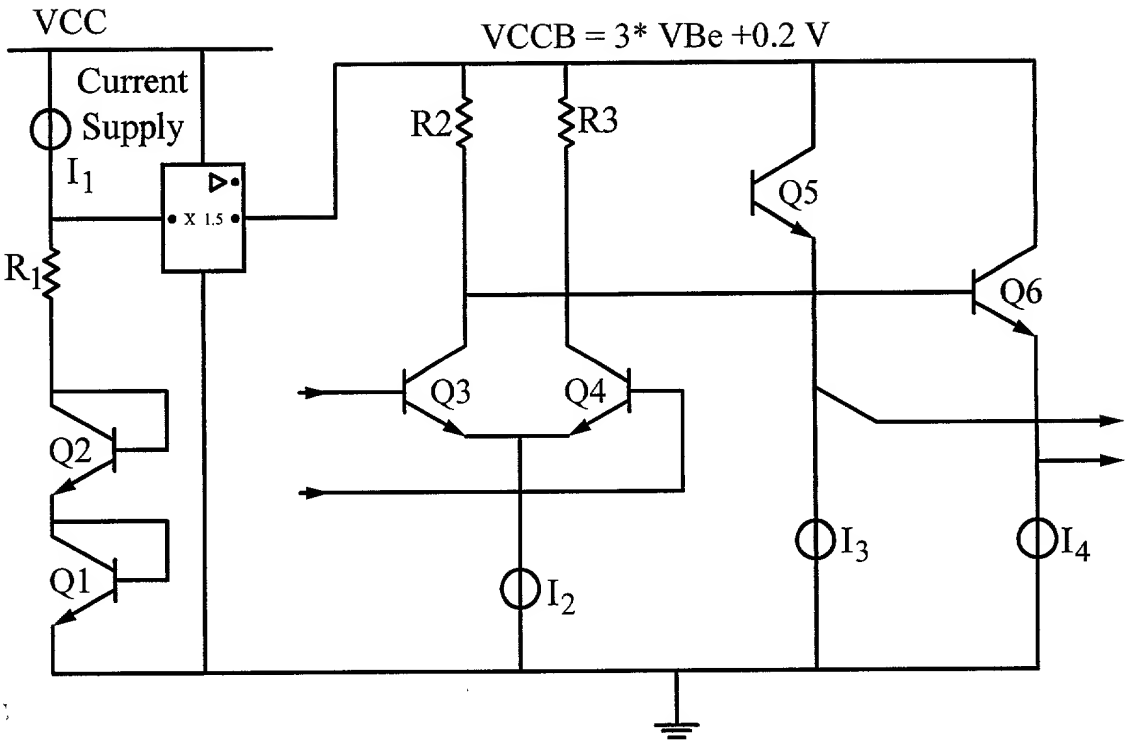
VCC
VCCB = 3* VBe +0.2 V
Current
Supply
I1
X 1.5
R1
R2
R3
Q5
Q6
Q3
Q4
Q2
Q1
I2
I3
I4

Fig. 6

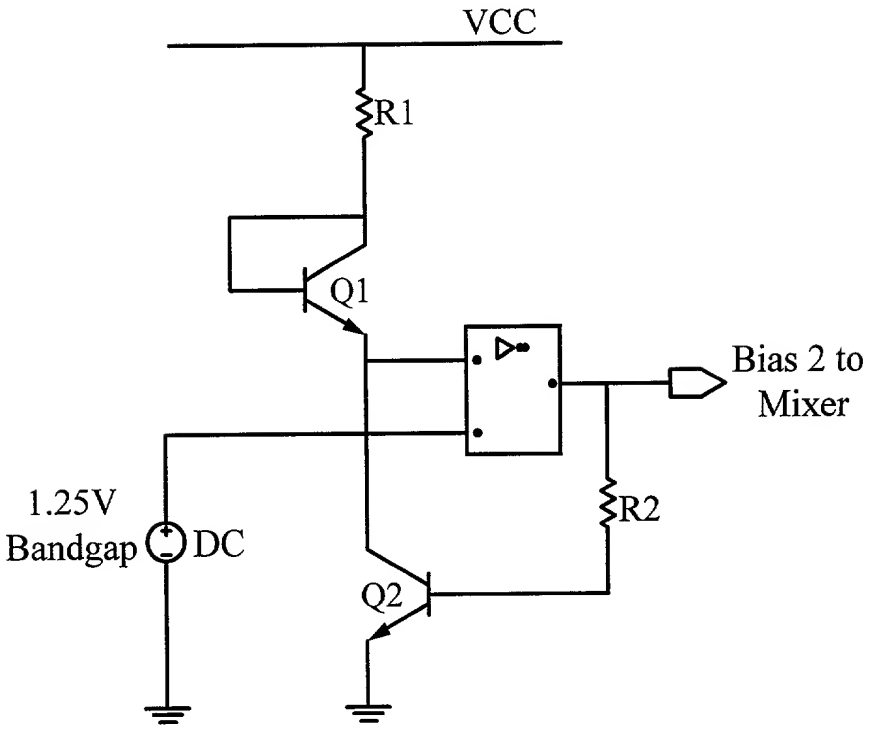

Fig. 7

EXPRESS MAIL LABEL #EL703212555US

Attorney Docket No.. PATENT
MLNR-0[illegible]
0810

DECLARATION FOR PATENT APPLICATION

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name. I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **NOVEL TOPOLOGY FOR A SINGLE ENDED INPUT DUAL BALANCED MIXER**. The specification of which is attached hereto). I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claim Yes	Priority Claim No
Number	Country	Day/Month/Year Filed		

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No	Filing Date	Status: Patented, Pending, Abandoned

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

60/167,188	November 23, 1999
Application Serial No.	Filing Date

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First Joint Inventor: Gwilym Francis Luff

Inventor's Signature: _____ Date

Residence: 18, The Hectare, Great Shelford, Cambridge CB2 5AT, United Kingdom
Citizenship: British
Post Office Address: 18, The Hectare, Great Shelford, Cambridge CB2 5AT, United Kingdom

Full Name of Second Joint Inventor: Selcuk Sen

Inventor's Signature: _____ Date

Residence: 1063 Morse Avenue #14-303, Sunnyvale, California 94089
Citizenship: Turkey
Post Office Address: 1063 Morse Avenue #14-303, Sunnyvale, California 94089